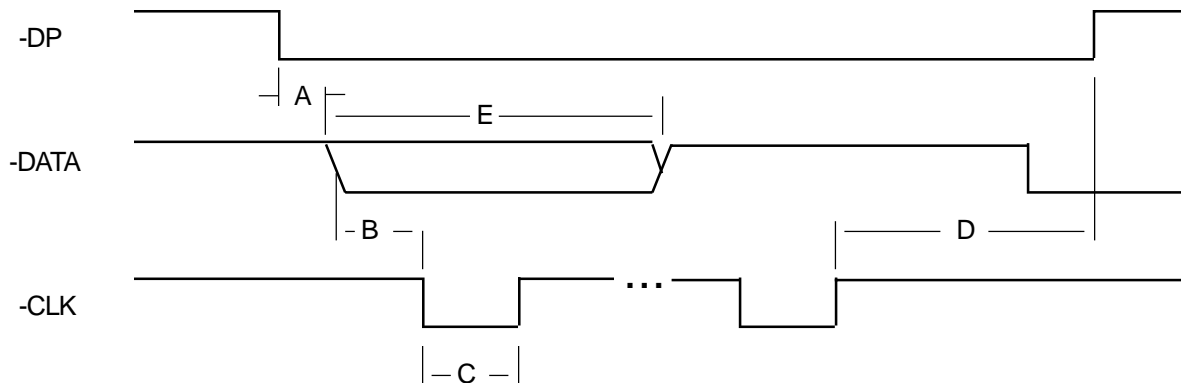


OUTPUT TIMING

- A 2ms MIN.
- B 2/3 BIT CELL LENGTH (E)
- C 1/3 BIT CELL LENGTH (E)
- D 18.4 to 36ms

Pin Assignment**1x7 7 pin**

PIN	SIGNAL	
1	+5V	
2	-DATA	Data bit Lo = Logic 1
3	-CLK	Clock LO data valid
4	-DP	Data present
5	-FCD	Front card detect
6	-RCD	Rear card detec
7	GND	